WHAT IS CLAIMED IS:

1. A method of extending the dynamic range of an electrical system including a variable gain amplifier connected to an analog-to-digital converter producing an output signal of predetermined bit-width, said method comprising:

receiving an analog signal of particular temporal magnitude;

amplifying the received analog signal by a first gain value;

changing said first gain value to a second gain value as a function of the temporal magnitude of the received analog signal;

converting the analog signal into a counterpart digital signal of predetermined bit-width;

modifying the counterpart digital signal with a selected one of predetermined offset values effective to ensure continuous linearity; and

adjusting the bit-width of the counterpart digital signal to compensate for a change in amplification provided by said variable gain amplifier.

2. The method according to claim 1 wherein an offset value corresponds to each trip-point in the slope of the ADC characteristic.

3. The method according to claim 1 including continuously extending the dynamic range of the electrical system, without abrupt variations.

4. The method according to claim 1 including producing an output digital signal indicative of

whether the analog signal detected exceeds a particular one of a plurality of predetermined thresholds and applying an offset corresponding to the particular threshold.

5. A processing system for an imager device comprising:

a camera system for producing an imager signal;

a correlated double sample circuit for receiving data from an imager;

a variable gain amplifier connected to said correlated double sample circuit, for receiving the sampled output of the correlated double sample circuit;

an analog-to-digital converter (ADC) coupled to said variable gain amplifier;

a shifter for holding a bit sequence of predetermined length, said shifter connected to the output of said ADC; and

a control circuit coupled to the output of said correlated double sample circuit and adapted to control the amplification setting of said variable gain amplifier, and to control the shift status of bits in said shifter, as well as to apply an offset value to correct a discontinuity in the gain characteristic.

6. A processing system according to claim 5, wherein said control circuit includes an analog-to-digital converter and logic circuitry for determining the values of offsets to be used in eliminating discontinuities in the gain characteristic.

7. A processing system according to claim 6, wherein said analog-to-digital converter includes a plurality of comparators connected to the output of said correlated double sampling circuit, which are used to

determine offset values used to eliminate discontinuities in the gain characteristic.

8. The processing system according to claim 7 wherein each of said comparators includes a positive input terminal connected to the output of said correlated double sampling circuit.

9. A method of correcting the extension of the dynamic range of an imaging system having a correlated double sampling system, a variable gain amplifier circuit connected to said correlated double sampling system, an analog-to digital converter connected to said variable gain amplifier circuit, and a shifter containing a predetermined number of bits greater than the digital output width of said analog-to-digital converter, said shifter connected to said analog-to-digital converter for receiving the output bit set of said analog-to-digital converter into predetermined locations in said shifter, including:

determining the magnitude of input signals from an imaging system, which are sampled by a correlated double sampling system;

adjusting the gain in a variable gain amplifier in a selected direction;

determining adjustment offset values corresponding to trip points at which gain adjustments are made; and

repositioning the bit set stored in said shifter in an opposite direction from the gain direction expressed upon said variable gain amplifier, to produce a digital output of greater dynamic range from said shifter than from said analog-to-digital converter.

10. The method according to claim 9 including detecting the magnitude of the output of said

correlated double sampling system to determine the adjustment of bit shifts in said shifter and the offset value to be added to the output of the ADC.

11. The method according to claim 9 wherein the VGA gain has a plurality of trip points with corresponding offset correction values.

12. A method of calibrating a dynamic range expandable imaging system having a correlated double sampling system, a variable gain amplifier circuit connected to said correlated double sampling system, an analog-to digital converter connected to said variable gain amplifier circuit, and a shifter containing a predetermined number of bits greater than the digital output width of said analog-to-digital converter, said shifter connected to said analog-to-digital converter for receiving the output bit set of said analog-to-digital converter into predetermined locations in said shifter, including:

injecting input test signals from a predetermined input circuit for sampling by a correlated double sampling system, above and below a first trip point in VGA input values at which VGA gain shifts have been determined;

determining the difference in analog-to-digital converter output corresponding to said first trip point;

injecting input test signals from a predetermined input circuit for sampling by a correlated double sampling system, above and below a next trip point in VGA input values at which VGA gain shifts have been determined; and

determining the difference in analog-to-digital converter output corresponding to said next trip point.

13. A trip-point correctable processing system for an imager device comprising:

a camera system for producing an imager signal;

a correlated double sample (CDS) circuit for receiving data from an imager;

a variable gain amplifier connected to said correlated double sample circuit, for receiving the sampled output of the correlated double sample circuit;

an analog-to-digital converter (ADC) coupled to said variable gain amplifier;

an offset injection mechanism (OIM) connected to said ADC for adjusting the output of said ADC;

a shifter for holding a bit sequence of predetermined length, said shifter connected to said OIM;

a control circuit coupled to the output of said correlated double sample circuit and adapted to control the amplification setting of said variable gain amplifier, and to control the shift status of bits in said shifter.

14. The processing systems according to claim 13 wherein said control circuit is coupled to said OIM to determine the amount of adjustment provided by said OIM.

15. The processing system according to claim 13 including a source of adjustment values.

16. The processing system according to claim 13 wherein said OIM is configured to apply a selected offset value as a function of the magnitude of received imager signals.

17. The processing system according to claim 13 including a mechanism for adding intentional offsets

to comparator inputs, which are used to control gain switching to ensure the VGA switches gain before the ADC saturates, whereby a digital output is enabled which is smooth and continuous during input level sweep changes.

18. The processing system according to claim 13 including a mechanism for calibrating dynamic range extension for ensuring removal of digital output discontinuities generable by analog domain gain switching disparities with respect to counterpart digital gain switching.

19. The processing system according to claim 13 wherein a potential offset error is generable by VGA analog gain change disparities with gain change shifts produced for offset adjustment.

20. A method to use an abbreviated bit ADC with a VGA and a simple small ADC to extend the dynamic range of the output while still maintaining low quantization noise at the low end of the signal range.

21. A method of adding intentional offsets to the comparator inputs that are used to control the gain switching in order to insure that the VGA switches gain before the output of the ADC saturates in order that the final digital output is smooth and continually changing as the input level is swept.

22. A method of calibrating the dynamic range extension circuit to remove any discontinuities that can be caused by gain switching in the analog domain which does not exactly match the gain switching in the digital domain.